

a3
~~input pad and a node and the internal circuit electrically connected to the node, the ESD protection structure comprising:~~

a3 concd
~~a single crystal Si resistor formed over an insulating material layer, electrically coupled between the input pad and the node; and~~

a3
~~at least a single crystal silicon-sided junction diode formed over the insulating material layer, wherein the single crystal silicon-sided junction diode is electrically coupled between one terminal of a corresponding power supply and a node.~~

Subt B²

a4
9. (Once Amended) An ESD protection structure having a single crystal Si-sided diode used to protect an internal circuit formed from an insulating material layer on a SOI, the ESD protection structure electrically connected between an input pad and a node and the internal circuit electrically connected to the node, the ESD protection structure comprising:

a4
~~an input resistor including a plurality of single crystal resistors formed over the insulating material layer, wherein each of the single crystal resistors is electrically coupled between the input pad and the node; and~~

a4
~~at least a single crystal sided junction diode formed over the insulating material layer, wherein the single crystal sided junction diode is electrically coupled between one terminal of a corresponding power supply and a node.~~

Sub A⁵
11. (Once Amended) The structure according to claim 9, wherein each of the single crystal resistors is made from a single silicon layer on the insulating material layer.

Please add new claim 21 as follows:

Subt B⁴

21. (Newly Added) An ESD protection structure used to protect an internal circuit, the ESD protection structure electrically connected between an input pad and a node, and the internal circuit electrically connected to the node, the ESD protection structure comprising:

a single crystal Si resistor formed on an insulating material layer, electrically coupled between the input pad and the node; and

a single crystal layer formed on the insulating material layer, wherein the single crystal layer comprises at least two doped regions with different dopant type to form a side junction diode, and the side junction diode is electrically coupled between one terminal of a corresponding power supply and a node.

REMARKS

Present Status of the Application

The Office Action rejected claims 1-20. Specifically, the Office Action rejected claims 1-20 under 35 U.S.C. 112, second paragraph. In addition, the Office Action rejected all claims 1-20 under 35 U.S.C. 103(a), as being unpatentable over Yamaguchi et al. (U.S. Patent 6,118,154) in view of Hu et al. (U.S. patent 6,121,077). Applicants have amended claims 1, 9 and 11 to overcome rejections under 35 U.S.C. 112, second paragraph. Applicants have also added independent claim 21. After entry of the foregoing amendments, claims 1-21 remain pending in the present application, and reconsideration of those claims is respectfully requested.

A marked up version of the amended specification paragraphs is attached hereto as Exhibit A, and a marked up version of the amended claims is attached hereto as Exhibit B.